Verigy Introduces SmartRA Redundancy Analysis Option for its V6000 WS Memory Test System

CUPERTINO, Calif., Jun 30, 2009 (BUSINESS WIRE) -- Verigy (NASDAQ:VRGY), a premier semiconductor test company, today introduced SmartRA (Scalable Memory Redundancy Technology), a memory redundancy analysis (RA) option for its V6000 WS test system. SmartRA provides a scalable, flexible, cost-effective solution that allows manufacturers to meet the expanding fail storage and performance requirements of redundancy analysis for DRAM. SmartRA will be showcased at the SEMICON West trade show in Verigy's Booth #921, South Hall, July 14 to 16, 2009 at the Moscone Convention Center in San Francisco.

Verigy's V6000 WS, introduced in November 2008, is the industry's first scalable, high-volume wafer sort test system for both Flash and DRAM applications. With SmartRA, V6000 WS users can easily add redundancy analysis capabilities for increased throughput and yield.

As DRAM device densities continue to increase, so do the challenges of today's wafer sort testing, requiring greater test parallelism, higher test frequencies and increased levels of complexity in device redundancy. These factors result in unprecedented volumes of data during redundancy analysis. Consequently, the storage and performance required to capture fail data and effectively complete redundancy analysis are also reaching new levels.

Verigy designed SmartRA to meet these requirements and because the solution utilizes high-performance blade servers, manufacturers can add processing power for redundancy analysis as they need it, without impacting the test cell footprint. SmartRA is based on an open software architecture which makes it possible for customers to use Verigy-provided algorithms or develop their own for faster time to market and lower cost-of-test.

"Unlike other testers that include the RA processing in the tester architecture, the V6000 with SmartRA doesn't require users to spend more on replacing hardware to maintain throughput and yield," said Gayn Erickson, Vice President, Memory Test, Verigy. "SmartRA's unique architecture and industry-leading throughput allow DRAM manufacturers to optimize their yield with scalable upgrades to provide the right performance at the lowest cost."

Hidden RA with SmartRA

SmartRA addresses the challenges of complex RA processes, including decreased throughput due to exposed RA time and decreased yields because of RA timeouts. The V6000 with SmartRA allows for increased throughput and yields by hiding RA time and eliminating pauses between patterns with changing test requirements.

About V6000

Verigy's V6000 family of testers addresses the entire semiconductor memory test process, including engineering, wafer sort and final test. The V6000 can test either Flash or DRAM memory by simply changing to a new test program and probe card, allowing manufacturers unprecedented flexibility to shift production volumes quickly and effortlessly between the memory types to meet market conditions and maximize profits. Verigy's V6000 testers include its patent-pending Active Matrix(TM) technology and sixth-generation Tester-Per-Site(R) architecture, which combine to deliver the industry's lowest cost-of-test. The Active Matrix technology provides massive parallelism, with over 18,000 I/O pins and over 4,000 programmable power supplies, and industry-best signal integrity due to a dramatically shortened signal path to pin electronics. For more information visit www.verigy.com/go/memory.

About Verigy

Verigy provides advanced semiconductor test systems and solutions used by leading companies worldwide in design validation, characterization, and high-volume manufacturing test. Verigy offers scalable platforms for a wide range of system-on-chip (SOC) test solutions, and memory test solutions for flash, DRAM including high-speed memories, as well as multi-chip packages (MCP). Advanced analysis tools accelerate design debug and yield ramp processes for Verigy's customers. Additional information about Verigy can be found at www.verigy.com.