



NOVELLUS

NOVELLUS DEVELOPS RESIDUE-FREE, 3X/2Xnm HIGH DOSE IMPLANT STRIP PROCESS

Innovative, CF₄-Based Approach Eliminates Photoresist Popping and Residues That Negatively Impact Yield

San Jose, Calif. - May 13, 2009 - As device performance requirements increase at the 3xnm technology node and beyond, the requirements for photoresist strip and clean are changing significantly. Shallower junctions and more abrupt gate electrode profiles are driving lower energy, higher dose implant steps, with doses typically in the $1E15\text{cm}^{-2}$ to $1E16\text{cm}^{-2}$ range. While these higher implant doses are necessary for improved device performance, they create challenges for photoresist removal such as the formation of thicker, cross-linked polymer "crusts" on the top surface layer of the resist, as shown in Figure 1.

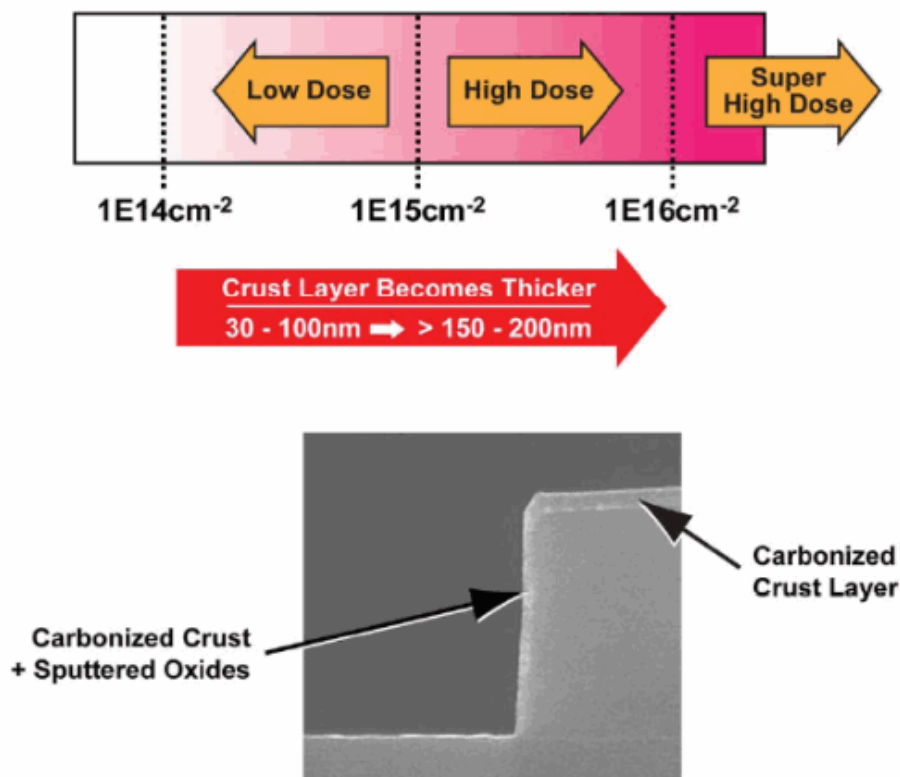
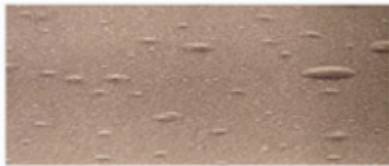


Figure1: Photoresist "crust" caused by high dose implants.

Rapid removal of this crust at higher temperatures can lead to resist "popping," a condition where solvents in the resist outgas through the crust and generate residues on the wafer surface, negatively impacting device yield (see Figure 2). After the crust is removed, the bulk resist is stripped away, and any remaining residues are cleaned from the wafer surface. Use of a fluorine-based chemistry such as CF_4 is the most efficient gas for this task; however, use of fluorine technology can be a challenge for some plasma-based systems requiring specific hardware modifications. In addition, the multiple temperatures and chemistries required for the High Dose Implant Strip (HDIS) process pose significant throughput challenges for strip systems based on single wafer process architectures.



Popping Residues
(strip temperature exceeds
resist bake temperature)



No Popping Residues
(strip temperature below
resist bake temperature)

Figure 2: Resist "popping" residue.

Confronting the challenges of HDIS integration at the 3x/2xnm node, Novellus (NASDAQ: NVLS) has developed a residue-free strip process using CF₄-based chemistries. The process runs on the GxT® photoresist strip platform that uses Novellus' multi-station sequential processing architecture (MSSP) to independently control chemistry and temperature at each process station. In the first step, the polymerized crust is removed, without popping, using an optimized process temperature. Subsequent stations, set to different temperatures, quickly remove the remaining resist and eliminate any residues from the wafer surface. No temperature or gas stabilization time is required between these steps, as would be required in a single wafer tool. MSSP enables the integration of optimized temperatures and chemistries for crust removal, bulk strip, and residue cleaning without sacrificing overall throughput. Figure 3 shows how residues are eliminated using Novellus' multi-temperature, CF₄-based solution in comparison to non-CF₄ approaches on the market. The GxT system has been engineered to be CF₄-tolerant, resulting in world-class defectivity levels under high volume manufacturing conditions.

"Higher dose implants are creating significant photoresist removal challenges at the 3x/2x technology node," said David Cheung, director of technology for the Surface Integrity Group at Novellus. "Novellus' optimized CF₄-based processes and MSSP architecture provide residue-free results, while providing industry-leading throughput for advanced HDIS applications."

For more information on 3x/2xnm residue-free strip processes, go to www.novellustechnews.com.

About Novellus' Photoresist Strip Technology:

Novellus' GxT system provides advanced photoresist strip technology for the most demanding applications, including low silicon loss, high dose implant strip, plasma assisted doping, and reducing chemistries required for back-end-of-line clean applications. The G400 for bulk photoresist strip features the highest productivity and lowest cost of ownership of any system on the market.

About Novellus:

Novellus Systems, Inc. (NASDAQ: NVLS) is a leading provider of advanced process equipment for the global semiconductor industry. The company's products deliver value to customers by providing innovative technology backed by trusted productivity. An S&P 500 company, Novellus is headquartered in San Jose, Calif. with subsidiary offices across the globe. For more information, please visit www.novellus.com

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