Outline

- Introduction
  - Interconnect Scaling Trend
  - Reliability Challenges

- Low k Dielectric Technologies
  - Bulk Low k Dielectric
  - Low k Dielectric Barrier
  - PSAB (Self Aligned Barrier)

- Cu Deposition Technologies
  - Scaling Barrier/Seed
  - Cu Plating/Anneal

- Cu Planarization Technologies
  - CMP (Dishing/Erosion)

- Summary
Benefits of Cu and Low k Interconnects

- Decreased RC Delay
  \[ RC \sim \varepsilon_0 \varepsilon_r L^2 (h^2 + w^2) \]

- Lower Power Consumption
  \[ P \sim CV^2f \]

- Reduced Crosstalk Noise
  \[ N \sim \frac{C_{L-L}}{C_{\text{Total}}} \]

Crosstalk \( \sim \frac{C_{L-L}}{C_{L-L} + C_{L-G}} \)

Line-to-line Capacitance = \( C_{L-L} \)
Line-to-ground Capacitance = \( C_{L-G} \)
Interconnect Scaling: Global vs. Local Wires

Global wires do not scale in length and thus more sensitive to RC delay.
Interconnect Delay vs. Technology Node
For ITRS Design Rules/Material Parameters

Reference: R. Ho & M. Horowitz

- Gate Delay (Fan out 4)
- Local (Scaled)
- Global with Repeaters
- Global w/o Repeaters

Global wire signal delay increases with scaling
Repeater insertion reduces global delay
Local wire signal delay improves with scaling
## Selected Interconnect Specifications from the ITRS

<table>
<thead>
<tr>
<th>Year</th>
<th>2005</th>
<th>2007</th>
<th>2010</th>
<th>2013</th>
<th>2016</th>
<th>2019</th>
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<tr>
<td>MPU ½ pitch</td>
<td>90</td>
<td>68</td>
<td>45</td>
<td>32</td>
<td>22</td>
<td>16</td>
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<td>MPU gate length (nm)</td>
<td>32</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
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<tr>
<td>Metal 1 barrier/cladding thickness (nm)</td>
<td>6.5</td>
<td>4.8</td>
<td>3.3</td>
<td>2.4</td>
<td>1.7</td>
<td>1.2</td>
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<td>Cu thinning at minimum Metal 1 pitch due to erosion (nm), 10% x height, 50% areal density, 500 um square</td>
<td>15</td>
<td>12</td>
<td>8</td>
<td>6</td>
<td>4</td>
<td>3</td>
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<tr>
<td>Interlevel metal insulator-effective dielectric constant (k)</td>
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<td>2.7 -</td>
<td>2.5 -</td>
<td>2.1 -</td>
<td>1.9 -</td>
<td>1.6 -</td>
</tr>
<tr>
<td></td>
<td>3.4</td>
<td>3.0</td>
<td>2.8</td>
<td>2.4</td>
<td>2.2</td>
<td>1.9</td>
</tr>
<tr>
<td>Minimum expected bulk dielectric</td>
<td>&lt;2.7</td>
<td>&lt;2.4</td>
<td>&lt;2.2</td>
<td>&lt;2.0</td>
<td>&lt;1.8</td>
<td>&lt;1.6</td>
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### New material/technology
- **R**: Barrier/Seed metal
- **R**: Cu Plating chemistry
- **RC**: CMP slurry/clean, control

### Manufacturability
- **Yellow**: Manufacturing solutions exist
- **Light Green**: Manufacturable solutions are known
- **Red**: Manufacturable solutions are not known

### New material/technology
- **C**: Bulk low k (porous)
- **C**: Dielectric barrier low k
**Cu Interconnect Evolution vs. Technology Node**

**Thinner Cu barrier & lower $k_{	ext{effective}}$ required**

- **130nm**
  - rf HCM PVD Barrier
  - HCM PVD Seed
  - FSG ($k \approx 3.6$)
  - SiN

- **90/65nm**
  - rf HCM PVD Barrier
  - HCM PVD Seed
  - Low $k$ ($k \leq 3$)
  - SiC

- **45/32nm**
  - HCM IONX™ Barrier
  - HCM IONX™ Seed
  - Porous Low $k$ ($k \approx 2.5$)
  - Cu Passivation
  - Cu Passivation
  - Cap/Etch Stop
  - Low $k$ SiC

- **22nm**
  - HCM IONX™ or iALD Barrier
  - HCM IONX™ or iALD Seed
  - Porous Low $k$ ($k < 2.5$)
  - Cap/Etch Stop
  - Refractory Cap

**Lowering RC requires new materials and processes**
Reliability Concerns for Copper Scaling

(1) Via reliability: Limits to scaling
Smaller features - larger stress gradients
Thinner barriers - less coverage, void nucleation

(2) Electromigration: Limits to scaling
Smaller features - less material to migrate
Thinner barriers - less barrier coverage
Increasing product J & EM requirements

(3) Dielectric Reliability: New concerns
Low k inter-level dielectrics - softer / lower $V_{BD}$, TDDB
Low k dielectric barriers: less hermetic
Electromigration (EM): a diffusion-controlled mass transport phenomenon
- Driving force: electron “wind” at high current density

Stress-induced back flow can counteract EM driving force
- Failures only occur on lines with length exceeding a critical value (Blech effect)

Two typical failure types: voiding and extrusion

Damascene Cu interconnects have multiple pathways for EM
- Cu / SiC interface. Dominant pathway when PVD process is robust
- Cu / Ta(N) barrier interfaces
- Cu grain boundaries

Electron Current or “Wind”

MTF ~ AJ^2 exp(Q/kT)
where  J = current density
  k = Boltzmann’s constant
  Q = activation energy
  T = absolute temperature

Source: Ogawa, IRPS 2002
EM Improvement Will be Needed at 45nm
Even if Jmax specification is constant

Scaling dimensions to smaller critical void volume requires significant EM improvement, further exacerbated by Joule heating effects.
Metal Cap Layers

**Metal cap layers**
- Ta(N), Co(WP), W

**Advantages:**
- Excellent Cu adhesion
- Low diffusivity (refractory metal, no EM)
- Current shunt of void (if thick)

**Disadvantages:**
- Increased line resistance
- Additional process

Metal cap layers reduce Cu interface diffusion & provide a current shunt
High Stress in Copper Interconnects
Byung-Lyul Park et al., IITC (2002)

First Thermal Cycle (passivation):
\[ \Delta \text{stress} \approx 250 \text{MPa} \]

Recrystallization:
\[ \Delta \text{stress} \approx 20 \text{MPa} \]

Grain growth: small contribution to stress
Cu stress fundamental to thermal expansion of Cu
Copper Creep: Stress / Diffusion Balance
E. Ogawa et al., IRPS (2002)

SM Model for Creep/Void-Formation Rate

\[
SM \ Model \ : \ R \propto (T_0 - T)^N \exp\left(-\frac{Q}{k_B T}\right)
\]

where: \( N \approx 3.2, \ Q \approx 0.74 \ \text{eV}, \ T_0 \approx 270 \ \text{°C} \)

- Stress gradient from \( \Delta T \)
  - Lower stress at higher \( T \)
- Diffusion of vacancies
  - Two competing elements

Fig. 3: McPherson and Dunn creep/voiding rate model.

Maximum void growth at \( \sim 200^{\circ} \text{C} \)
Stress Migration Void Growth Depends on Cu Volume

No SM failures if Cu volume under (or over) via is small; failure rate increases with more Cu below (or above) via.

Fig. 3: Cumulative failure by using the test pattern A. The SIV failure has occurred with metal length dependency, as metal width is more than 10μm. However, cumulative failure has been saturated, as metal length is longer than 50μm.

Fig. 1: Voids are formed under the via when the via connects to a wide metal line below it [1].
Cu/low k Interconnect Technologies

- Bulk low-k
- Dielectric Barrier
- Barrier/Seed
- Cu Plating
- CMP
ULK Integration Requirements

- Learning based on development of 90nm low k dielectric
- **High film modulus** improves adhesion and CMP performance
- **High film cracking limit** improves integration and packaging performance
  - Film cracking limit is related to film modulus ($M$) and stress ($\sigma$)
- Cohesive strength is proportional to $M/\sigma^2$

Key CDO film mechanical property--cohesive strength--is related to $M/\sigma^2$
**Scaling the Bulk Low k Dielectric**

- **Low k dielectrics required for capacitance scaling, but:**
  - Weaker electrical and mechanical properties are a concern
    - UV Thermal Processing (UVTP) improves film modulus
  - High porosity of Ultra low k (ULK) films presents integration issues
    - Reduced pore interconnectivity enables standard process for lower cost

![Graph showing RC delay vs Wafer Split ID for HMS (k=3) and ULK (k=2.5)]

**Closed pore ULK with UVTP enables lower RC and process cost**
UVTP Tuning of Dielectric Constant and Hardness

1. Porogen removal is the dominant step. Both $k$ and $H$ decrease.

2. Porogen removal + Cross-linking. Stable $k$, hardness increase.

3. Porogen removed, Cross-linked structure formed, $k$ increases slightly, increased $H$.

UVTP enables ULK Coral™ of $k < 2.5$ with Hardness $> 1.1$ GPa.
Cu/low k Interconnect Technologies

Dielectric Barrier

Bulk low-k

Barrier/Seed

Cu Plating

CMP
Scaling $k_{\text{effective}}$ of the Low $k$ Dielectric Barrier

**Issues:**

- **Low $k$ SiC**
  - Hermeticity
  - Etch selectivity
  - Hardness/Modulus

- **SiCN**
  - Higher $k$

**Combined performance**

- SiCN-Cu interface
- Superior electrical performance
- Hermetic film stack
- Excellent diffusion barrier properties
- Excellent etch stop

**Integration Requirements**

- Interface control and process repeatability
- Etch profile control and process integration

SiCN/low $k$ SiC bilayer provides best combined $k_{\text{effective}}$ & performance
Making a Reliable SiC Diffusion Barrier

Resistance to moisture and oxygen

H₂O absorption in damaged CDO leads to the formation of Cu₂O.

- Permeable SiC
- Hermetic SiC

Dielectric Constant

- Permeable SiC: 2.7, 2.9, 3.1, 3.3, 3.5, 3.7
- Hermetic SiC: 3.1

Interfacial O (atoms/cm²)

- No Cu₂O Reduction
- Permeable SiC
- Hermetic SiC

% Adhesion Failures (<5 J/m²)

- No Cu₂O Reduction
- Permeable SiC
- Hermetic SiC

Hermeticity of the dielectric barrier is key to Cu/low k reliability.
Improving Dielectric Barrier Reliability

Device reliability improves with longer wafer heat-up time

Cu Line-to-Line Leakage

1x Heat-up Time Before SiC dep
3x Heat-up Time Before SiC dep

Split ID
Plasma Self Aligned Barrier (PSAB) Process Sequence

The Vector platform enables this application

- PSAB process optimum at < 300° C
- Deposition at 350 to 400° C
- PSAB on station 1, Deposition on stations 2,3,4

PSAB offers low cost solution for interconnect reliability improvement
Interface Engineering: \( \text{Cu}_x\text{Si}_y \) Formation
M. H. Lin et al., IRPS 2004

- **Formation of \( \text{Cu}_x\text{Si}_y \) layer at interface = improved EM (2x)**

**Fig. 7** High magnification TEM image on Cu/Cap interface. Cu-siliside (\( \text{Cu}_x\text{Si}_y \)) formation between Cap/Cu interface is proposed to be a EM enhancement mechanism.

- \( \text{Cu}_x\text{Si}_y \) alloy layer:
  - Good adhesion
  - Shunts current away from interface
  - Increase in resistance from Si in bulk

- **2x EM Improvement**
- **10% resistance increase**

**CuxSiy layer**
**Cu Barrier/Seed**

- **Lower line resistance achieved by optimizing Cu volume:**
  - Requires thinner barrier while maintaining barrier integrity

### Graph

- Effective Resistivity ($\mu \Omega \cdot cm$) vs. Line Width (nm)
- 25nm PVD (Conventional PVD)
- 10nm PVD (RF HCM PVD)

### Diagram

- "Quasiconformal"
- RF HCM TaN

**RF HCM PVD barrier extendable to 32nm node; iALD offers further extendibility**
HCM utilizes well known magnetron effects

Diode Sputtering

\[
\text{Ar} + e \rightarrow \text{Ar}^+ + 2e^-
\]

Magnetron Sputtering

\[
\text{Ar} + e \rightarrow \text{Ar}^+ + 2e^-
\]
Hollow Cathode Magnetron (HCM)
Directional Metal Ion Deposition

Metal ions ($M^+$) follow electrons along magnetic field lines to plasma sheath
- Partial directionality in bulk plasma

Metal ions accelerate across plasma sheath resulting in directional deposition
- Most directionality occurs in collisionless sheath

\[ \Delta \Phi = V_p - V_t \]

\[ V_p > 0 \]

\[ V_t < 0 \]
Electron confinement via Separatrix

- Formation of ‘magnetic mirror’ at opening of HCM prevents electron loss and results in high density plasma
HCM IONX™ PVD Technology

**Enabling Hardware**
- Ion Extractor
- Pedestal Electromagnet

**On-Wafer Benefit**
- Film morphology
- Step coverage / overhang
- Film density
- Process uniformity
- Soft etch

**HCM Design Concept:**
- Independently generate metal and Ar ions
- Ion flux uniformity controlled by electromagnets
- Simple design: Single piece target in the plasma
PVD: HCM IONX™ Barrier Step Coverage Enhancement

1. Barrier Deposition (Ta/TaN)

2. RF Biased Ar⁺ Etch / Ta Deposition

As deposited

After resputtering
Barrier First Integration Scheme

**Advantages of Barrier First Approach:** No low k damage \((k\text{-shift, CD loss/faceting, adhesion loss})\), no Cu contamination of dielectric.
Reactive Preclean + Barrier First Integration Scheme

Benefits of reactive preclean
- Improved via cleaning
- Effective cleaning of M1 level trench

Benefits of Barrier First
- Via anchoring to improve reliability

Reactive Preclean + Barrier First approach improves process margin when previous via strip and clean steps are not robust
PVD Ta(N) Barrier Optimization
HCM IONX™ Ta(N)

Minimize Barrier Thickness (Line Rs)
TaN Oxidation Resistance, Adhesion
TaN Wettability
Low Overhang
Via
Smooth Continuous Morphology, High Density
Barrier Thickness (SM/EM Reliability)
Anchor with Trench Protection, No Micro-trenching (Selectivity)

HCN IONX™ Ta(N) barrier has high density and quasi-conformal step coverage
HCN IONX™ Cu seed has good morphology/step coverage with low overhang
**Ion Induced Atomic Layer Deposition (iALD)**

1. **Precursor Adsorption**
   - ALD schemes are differentiated by the technology used in steps 1 and 2.
   - Adsorption/Reaction technologies have dramatic affect on film properties and process performance.

2. **Reaction / Ligand Removal**

   ![Diagram showing the process of ion-induced atomic layer deposition](image)

**iALD provides conformal, high density, low resistivity films**

IALD technology is used to deposit TaN, Ru and Cu.
**iALD TaN Film Properties**  
**Key Differentiators vs. Thermal ALD**

**Key Film Attributes**
- High density: >13 g/cm³
- Low resistivity: <300 μΩ·cm
- Conformal, uniform film

![Film Resistivity vs. Thickness](image)

Resistivity (μohm-cm) vs. Film Thickness

- **Typical Thermal ALD**
- **PVD TaN**
- **iALD TaN**

**iALD TaN** is a conformal low resistivity high density barrier
iALD TaN Integration & Reliability

C vs. 1/R

1.00E-11 1.25E-11 1.50E-11
1.00E-11 1.25E-11 1.50E-11

13% reduction in R

PVD

iALD

M2 line at 350°C
500µm long, 0.2µm wide
0.14µm via

Wafer Level EM

Time to Fail (s)

20A iALD TaN BKM3 + PVD Ta
20A iALD TaN BKM4 + PVD Ta
PVD Baseline

iALD TaN + PVD Ta flash bi-layer provides lower line resistance and equivalent electromigration reliability to standard PVD Ta(N) barrier
Cu/low k Interconnect Technologies

- Dielectric Barrier
- Bulk low-k
- Barrier/Seed
- Cu Plating
- CMP
Evolution of Damascene Cu Challenges

Development Timeframe


Requirements

Fill capability
130 nm

Planarity
90 nm

Faster fill
45 - 65 nm

Reliability
32 nm

Nucleation across resistive films
22 nm

Fill: Electrolyte composition
Fill: Suppressor gradient
Purity modulation

Early Cu baths based on PWB chemistries
Accelerator accumulation based fill
Levelers with low fill impact
Improved levelers and stronger suppressors
Plate on Barrier
Conformal Seed

PVD barrier and Cu seed of decreasing thickness
Challenges for Cu fill of smaller feature size:

- Smaller features require faster bottom-up fill without overplating
- Must compensate for nonuniform current distribution from thin Cu seed

New plating chemistry & tool enhancements enable Cu fill extendibility
Electrolytic Copper Deposition Cell
Fundamentals

$$\text{Cu}^{2+} + 2e^- = \text{Cu}(0)$$

One Cu atom deposited for every two electrons delivered.
Electrofill Process Cell

- Cathode (Wafer)
- Wafer mounting hardware
- Electrical Contacts
- Anode Chamber
- Membrane
- Copper Anode
- Membrane
- Plating Solution
Role of Chemical Additives in Bottom-up Fill

- **t = 0 sec**: Wafer immersed in plating bath. Additives not yet adsorbed on Cu seed.
- **t = 1 sec**: Additives adsorbed on Cu seed, little plating has occurred.
- **t = 3 sec**: Conformal plating started in feature; accelerating species accumulate near base.
- **t = 10 sec**: Rapid growth near base occurs as accelerators accumulate due to decrease of surface area inside feature.
- **t = 20 sec**: Fill is complete, Cu over feature has an adsorbed excess of accelerating mercapto species.
- **t = 60 sec**: Deposition following fill with levelers or accelerator desorption.
- **t = 60 sec**: Deposition following fill without levelers or accelerator desorption.

- **L**: Levelers: Current suppressing additive with mass transfer sensitive distribution on wafer surface.
- **C**: Suppressors: Polymer additive which forms current inhibiting film on Cu. Enhances wetting.
- **c**: Chloride ion
- **Lc**: Accelerators: Organic sulfide which negates suppressor impact by catalyzing Cu reduction.
Fill Evolution vs. Feature Size

Fill begins first in small features and sequentially initiates in increasingly large features.
Ideal Leveler Behavior During Deposition

A.) Non-leveling suppressor

B.) Leveling additive present

Growth rate in and over feature

Cu Growth rate

Field growth rate

Fill complete

Deposition complete

Time

Accelerated Cu growth continues over features without levelers; levelers reduce overgrowth after filling
Fast fill acceleration in small features requires strong suppression of field current using polymers which diffuse slowly into features.
Key Issues With Seed Thickness Scaling

- As device geometries shrink, the seed thickness needs to be scaled.
- The use of copper as a seed may give way to materials like ruthenium.
- This leads to a “terminal effect” where thickness distribution is less uniform as the seed resistance increases.

Thickess distribution on thin seeds requires terminal effect compensation.
Terminal Effect Compensation with Thin Cu Seed
High Resistance Virtual Anode (HRVA)

Plating Bath Equivalent Circuit

Power Supply

Electrolyte

Membrane

Anode

Wafer

Edge

Center

$R_{\text{wafer}}$

$R_{\text{electrolyte}}$

$R_{\text{HRVA}}$

$R_{\text{HRVA}}$

$R_{\text{HRVA}}$

$R_{\text{HRVA}}$

Thickness Uniformity with and without HRVA

Seed Thickness

Thickness RSD (%)

0 3 6 9 12 15 18

Standard Cell

HRVA

Increased plating cell resistance with HRVA compensates for terminal effect caused by highly resistive Cu seed.
Line Width Dependence of Cu Resistivity

Electron Scattering Effects

Surface & Interface Scattering
(specular or diffuse $0 < P < 1$)

Grain Boundary Scattering
$(0 < R < 1)$

Grain boundary scattering dominates resistivity; larger grains = lower $\rho$
Optimization of Cu Resistivity

**Cu resistivity increases with smaller feature size:**
- Electron scattering from grain boundaries and sidewalls
- Optimized chemistry/anneal gives large grain size & lower resistivity

**Copper Anneal/Plating Chemistry**
Optimized for Large Grain Size

Lower effective Cu resistivity with optimized plating chemistry & anneal
Cu/low-k Interconnect Technologies

- Dielectric Barrier
- Bulk low-k
- Barrier/Seed
- Cu Plating
- CMP
Cu Planarization

Cu planarization impacts both performance (RC) and yield:
- Dishing impacts R and erosion impacts C - polishing control is key
- Post-CMP clean must be optimized for low defects (and low k films)
- ULK dielectrics require lower shear force processing

Pre-CMP Challenges:
- ECD Overplating
- Faceting
- ECD Dip
- Underlying Topography

Post-CMP Issues:
- Erosion
- Residue
- Corrosion
- Scratches
- Protrusion
- Dishing
- Particles
- Adhesion
- Failure

Good polishing control and post-CMP clean are critical to performance & yield
CMP Productivity Improvement

**Momentum/Xceda**

Through the Pad Slurry Delivery

- Enables Direct Delivery of Slurry to the Wafer Surface
  - Improved Control of Chemical Uniformity
  - Lowest Slurry Usage

**Conventional Rotational**

On Pad Slurry Delivery

- Constraints Force Indirect Slurry Delivery: Pad->wafer
  - No Chemical Control on the Face of the Wafer
  - Slurry Wasted on Large Pad
Endpoint/uniformity control are critical for Cu scaling:

- Performance (RC) depends upon final Cu thickness
- Tighter control needed as devices scale due to thinner Cu

Good polishing control is key to performance & yield of Cu interconnects
CuVision™ Real Time Control

Real Time Pressure Zone Control

Control Computer

Real Time Measurements from Eddy Current Probes

Data From Removal Profile

Real Time Process Control for WiW/WtW Consistency

Cu Thickness (Å)

Pre st.dev. 915Å

Post st.dev. 143Å

Wafer Diameter (mm)
Summary

- Device performance requirements continue to pace the need for new BEOL materials and processes
  - Ultra low k (k <2.5) dielectrics and lower k dielectric barriers
  - Thinner low resistivity Cu barriers / more conformal seed
  - Faster fill plating chemistries / plating on higher resistance seed
  - Low shear force CMP with low defect slurries & post-CMP cleans

- “Nano-engineered” solutions will likely be needed to address future scaling and performance challenges beyond 32nm
  - Mechanically robust porous ELK materials
  - Low k dielectric barriers and/or self-aligned barrier
  - iALD barrier/seed
  - Faster, void-free Cu fill and plate on highly resistive seed
  - Low damage CMP with low defectivity post-CMP clean
  - Process uniformity and repeatability will pace future scaling

- Tradeoff between performance and reliability is a looming challenge for 32nm and beyond
  - Smaller critical volume
  - Joule heating effects
  - Increase in resistivity from electron scattering