Stress Migration and the Mechanical Properties of Copper

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ABSTRACT

Variations in the mechanical properties of copper related to plating chemistry and copper thickness are found to control stress migration performance in dual damascene copper interconnects. These observations cannot be explained by vacancy diffusion alone. Instead, the high tensile stress of the copper and elastic vs. plastic energy dissipation needs to be considered to account for the degradation in stress migration.

INTRODUCTION

High temperature processing of copper dual damascene structures leaves the copper with a large tensile stress due to a mismatch in coefficient of thermal expansion of the materials involved. The stress can relax with time through the diffusion of vacancies leading to the formation of voids and ultimately open circuit failures. [1, 2, 3] Controlling this phenomenon requires optimization of several processes including copper annealing, [4] metal barrier deposition process, [5] and interconnect geometry. [6,7] In this paper, it is shown that variations in the plating chemistry and the underlying metal thickness can modulate the stress behavior of copper, which has an impact on via stress migration. Copper with a low yield stress is found to give superior stress migration performance due to the plastic dissipation of local stress in the copper.

EXPERIMENT

A two metal layer test structure was fabricated using conventional 180nm node technologies and SiO₂ as the interlevel dielectric with SiN as the copper capping layer and etch stop. The concentration of organic additives in the copper-plating bath was varied to modulate the microstructure and physical properties of the copper. Both metal 1 and 2 used the same copper plating process and a post plate anneal condition of 150°C for one hour prior to CMP. Stress migration was characterized by measuring the resistance shift of single vias after a cyclic anneal from 150°C to 250°C. [8] The vias were 0.25μm in diameter with a 12 μm contact area of copper above and below the via. Three wafers were used for each experimental cell with 120 vias per wafer measured. The PVD barrier process used for this work had an aggressive Ar sputter preclean that is known to enhance stress migration failures. [4] The stress migration failure mode induced by this aggressive Ar sputter etch is a void in the Metal 1 layer under the via due to poor adhesion at the metal / dielectric interface. An alternative barrier process can reduce this effect by depositing a TaN barrier metal layer first and then performing the sputter clean such that respattered copper is deposited on TaN and not a dielectric. This process improved the stress migration performance as shown in Figure 1. For the purpose of this study, we used the Ar sputter clean process with a large stress migration signal to magnify the effect of copper chemistry.

RESULTS AND DISCUSSION

Via stress migration results for three different plating chemistries are shown in Figure 2. A degradation of stress migration performance is observed for chemistries 2 and 3 relative to chemistry 1. Analysis of the microstructure for copper deposited with each chemistry was done by FIB/SEM.

![Figure 1: Resistance shift of an isolated Kelvin tester with two methods of via cleaning. The Ar sputter method leaves copper on the side walls of the via degrading adhesion.](image1)

![Figure 2: Resistance shift of an isolated Kelvin via tester for copper plated with three different chemistries.](image2)
and X-ray diffraction. Grain growth in the copper was complete after the post-plate anneal of 150°C and the 400°C dielectric deposition. No grain growth is expected during the thermal treatment used to induce stress migration. Both blanket films and the Kelvin stress migration testers showed smaller grains for chemistry 1 (Figure 3) relative to chemistry 3 (Figure 4). The grain size was similar for chemistries 2 and 3. The observation of a smaller grain size but improved stress migration performance for chemistry 1 relative to chemistry 2 and 3 is contradictory to the model of void formation from the coalescence of vacancies from grain boundaries in the copper. [4] A high concentration of vacancies at the grain boundaries is required to account for the void volume that forms under a via. Smaller grains should increase the availability of vacancies and degrade via stress migration. However, we observe the opposite trend for copper deposited with chemistry 1 relative to chemistry 2 and 3.

The mechanical properties of the different copper films were examined by stress-temperature curves. [9, 10] Stress-temperature hysteresis is very useful in understanding the properties of electroplated copper. Figure 5 shows a typical stress vs. temperature curve for a blanket 0.8µm film on 150nm of copper seed and 25nm Ta(N) barrier. As deposited, the film had 50-100MPa of tensile stress. Upon heating, the tensile stress is reduced due to the larger coefficient of thermal expansion for copper relative to Si. At a temperature of ~150°C, there is an increase in the copper tensile stress. This is the same temperature at which recovery/recrystallization of the copper occurs on the time scale of the ramp rate. Copper that has undergone recrystallization at room temperature before being heated does not show this inflection point in the stress. The tensile stress increases in the copper due to a reduction in vacancy and grain boundary concentration. It is important to note that the change in stress associated with recrystallization is ~ 40 MPa for this thickness of copper. The change in stress of the copper after the full temperature cycle is 200MPa. Therefore the dominate source of stress in copper films is the differential thermal contraction of the copper and not grain growth and recrystallization.

To make a quantitative comparison of the mechanical properties of copper, samples were prepared that best mimic the copper in encapsulated features. Copper films 0.8µm thick were deposited from chemistries 1 and 3 on blanket wafers with a 25nm Ta(N) barrier and 100nm copper seed film. The copper was then annealed at 150°C for 1 hour for recrystallization and then polished back by CMP leaving a
final Cu thickness of 0.7µm. The blanket wafers were then passivated with a 70nm SiN film and a 1µm of TEOS oxide at a deposition temperature of 400°C. The mechanical behavior of these passivated blanket copper films should be similar to the behavior of fully encapsulated wide copper lines such as those used in a stress migration testers. [3, 10] The absolute value of the stress in the copper is difficult to isolate from the stress in the dielectric above and below the copper, so values shown are in arbitrary units. Several heat/cool cycles were performed on the wafers to isolate the kinematic yield properties of the copper from dynamic yield properties such as work hardening. [11] The inelastic properties of copper films during a thermal cycle have been attributed to bulk deformation and interface controlled dislocation glide [9] or diffusional creep [10]. Figure 5 shows that the stress-temperature curves are very different for copper deposited with chemistry 1 relative to chemistry 3. The hysteresis curves are controlled by the yield stress of the copper. The yield stress can be inferred from the change in slope in the stress-temperature curve. [10] Differential thermal contraction of the copper relative to SiO₂ should have only one slope until the tensile stress of the copper exceeds the yield stress. At the yield point, the copper deformation becomes inelastic [9] and the slope of the stress-temperature curve changes to track the yield stress vs. temperature dependence. The hysteresis loop for the copper deposited with chemistry 1 is smaller due to a lower yield stress of the copper relative to chemistry 3. However, even with a difference in the yield points for the copper, the absolute stress level at ambient and at the stress migration temperatures of 200-250°C are similar for the two copper films. Therefore, the stress level alone cannot account for the stress migration difference.

The above observations would indicate that there is a correlation between the yield properties of copper and stress migration. Copper with a lower yield stress (more ductile) has better stress migration performance than copper with a high yield stress (less ductile). An alternate method of modulating the stress of a copper film is to change the thickness. [12] For example, Figure 6 shows that the stress in a copper film after a thermal cycle to 350°C increases as the thickness is increased. This phenomenon has been documented previously and is due to an increasing volume of copper that can deform as thickness is increased. [10, 12] Adhesion measurements with 4-pt bending show that copper films thicker than ~200nm have more volume available to plastically deform resulting in higher adhesion energies relative to thin copper films. [14]

Experiments were performed in which the metal 1 thickness was varied from 0.5µm to 0.1µm to modulate the stress of the.
copper. All other dimensions of the via remained unchanged. The stress migration performance degraded substantially with reduced metal 1 thickness as shown in Figure 7. Failure analysis showed that the post anneal stress voids were larger in the 0.1µm film and formed along the SiN / copper interface as shown in Figure 8. The absolute via resistance did not change significantly with the reduced metal 1 thickness because the spreading resistance of the lower copper film is a small contribution to the total via resistance relative to the high resistivity barrier material at the bottom of the via. This result is opposite to the generally observed trend of improved via stress migration with reduced copper volume under a via due to fewer available vacancies. [4, 6] It would appear that stress gradients in the copper dominate the stress migration performance over the absolute number of vacancies.

Finite element analysis was performed of the stress levels in the copper within a confined via structure to understand how copper thickness and yield stress could affect via stress migration. All stress levels of the copper were set to zero initially and the structure was cooled by 200°C to simulate a thermal cycle from 400°C to 200°C. The largest thermally induced stress gradient in the copper were at the lower corner of the via at the SiN etch stop layer as shown in Figure 9. This is the same location where we observe nucleation of voids after stress migration tests as shown in Figure 8. [4] If we assume that these voids are due to the initiation of cracks or adhesion failure at the copper / SiN interface then the elastic and inelastic energy release rate can be calculated for copper with different yield stresses and thickness. [11] Two extreme examples were considered. A 0.1 µm thick layer of copper should have a yield stress of ~920 MPa and was found to have an elastic energy release rate of 10 mJ/m² but a plastic energy release rate of less than 0.1 mJ/m² for a 30nm crack initiation. Therefore, the thick copper with a low yield stress had a lower plastic energy release rate and was therefore able to absorb the strain energy through plastic deformation without forming a crack.

Finite element calculations show that an increase in the thickness and / or a decrease in the yield stress of copper allows strain energy to be dissipated in the copper without forming a crack. If the yield stress of the copper is high, then the stress energy in the copper will go into the formation of a crack at the copper / SiN interface in the corner of a via. Once the crack is initiated, it can grow into a void through vacancy diffusion. The energy release rates calculated here are smaller than what is typically observed in 4-point bending adhesion measurements, but the length scales for the finite element calculations are 1E-9 m whereas 4-point bending test are done on a mm length scale. The absolute values of the calculated crack energies also depend strongly on the radius of curvature at the via bottom and the crack length used for the calculation. Therefore, a high degree of quantitative agreement between the finite element calculations and experimental 4-point bend values would not be expected.

Stress migration behavior that scales with the yield stress of copper is consistent with void formation that occurs through an elastic volume contraction of copper under high tensile stress. The size of a void (δV) that can form through contraction of a volume of copper V under a via would be given by

\[ \delta V = \frac{V \sigma}{E} \]  

where  \( \sigma \) is the local stress and  \( E \) is the modulus. Contraction of a ~30µm³ volume of copper under a via with a stress level of 300MPa would correspond to a void volume of ~0.1µm³. This is similar to voids that are observed after a stress migration test. Therefore, much of the initial volume associated with a void could be due to simple thermal contraction and not vacancy diffusion. However, growth of the void would have to occur through vacancy diffusion with the characteristic temperature dependence that has been observed. [4] The vacancy concentration required to form a void from supersaturation of vacancies is larger than what is required to grow a pre-existing void. If there are no pre-existing voids and if the stress gradients in the copper are such that vacancy supersaturation does not occur, then there would be no stress migration induced failures because no voids could nucleate. If the local adhesion energy between the copper and barrier and the dielectric are lower at some location than the yield stress of the copper then a voids can nucleate due to poor adhesion with a volume given roughly by equation (1).

The stress migration results of Figure 1 demonstrate that there is a strong dependence of stress migration performance on the metal barrier process and pre-clean. [4, 6, 7] This is consistent with the critical dependence of metal/dielectric adhesion on stress migration performance in addition to copper grain structure. [4] The via pre-clean and PVD barrier deposition process would not have any impact on copper grain
structure yet there is a major impact on stress migration performance.

**CONCLUSION**

In conclusion, we have shown through a combination of chemistry variation, copper thickness variation and finite element calculation that the stress migration performance of copper dual damascene structures depends on the yield stress of the copper in the interconnect. Initiation of a void at the corner of a via is controlled by the high stress level of the copper after a thermal cycle. Once void initiation occurs, vacancy diffusion can cause the void to grow. Therefore, one of the most critical elements for the control for via stress migration in copper dual damascene interconnects is the elimination of nucleation sites for voids in a via through improved metal/dielectric adhesion.

**REFERENCES**