



## Magma's Talus IC Implementation System Included in TSMC Reference Flow 10.0 Targeting 28-nm Process Technology

### New Bottom-Up Hierarchical and Hotspot Fixing Flows Improve Performance, Power and DFM

SAN JOSE, Calif., July 27, 2009 (GLOBE NEWSWIRE) -- Magma(r) Design Automation Inc. (Nasdaq:LAVA), a provider of chip design software, today announced that the Talus(r) IC implementation system has been included in [TSMC Reference Flow 10.0](#). With [Magma](#) software and the latest TSMC Reference Flow, designers have access to the "Fastest Path to Silicon(tm)" for designs targeted at TSMC's 28-nanometer (nm) processes.

"TSMC 28-nm processes offer the promise of billion-gate ICs, but also bring the challenge of dealing with more physical effects, tougher power requirements and difficult timing closure issues," said Premal Buch, general manager of [Magma's](#) Design Implementation Business Unit. "[Magma's](#) latest release, [Talus 1.1](#) with our new COre(tm) technology, combined with TSMC's Reference Flow 10.0, provides faster design closure on large, tough designs."

COre is [Magma's](#) new Concurrent Optimizing routing engine. This new routing engine, which includes the ability to push critical wires to a thicker and wider metal layer, supports TSMC's 28-nm design rules and provides faster overall design closure with better performance and predictability.

"For years TSMC has been leveraging close collaboration with leading EDA vendors, such as [Magma](#), to co-optimize EDA design technology and our advanced process technology," said S.T. Juang, senior director of Design Infrastructure Marketing at TSMC. "With the inclusion of the Talus system for Reference Flow 10.0, TSMC and [Magma](#) offer mutual customers differentiated design and process technologies that improve power, performance and design for manufacturability of 28-nm ICs."

### Enabling 28-nm Design through the Open Innovation Platform (OIP)

Through the OIP and Active Accuracy Assurance initiative, TSMC enables innovation by promoting quality and accuracy throughout the semiconductor ecosystem. [Magma](#) software has supported the OIP since the platform's inception. [Magma](#) works closely with TSMC and mutual customers early in the R&D process to ensure product enhancements satisfy customers' deployment requirements. By engaging with TSMC and customers early, [Magma](#) has ensured that Talus is able to implement designs targeted at TSMC's 28-nm processes.

### Enhanced Low-Power Design Techniques

Low-power support in Reference Flow 10.0 has been expanded to include the bottom-up hierarchical Unified Power Format (UPF) flow. The UPF can be used to specify low-power design techniques at all levels of a hierarchical design flow. For low-power flows with multiple voltage islands, support for disjoint power domains with dual power SRAMs is now available. To address leakage, Talus is able to optimize leakage at different corners from timing optimization. This provides more accurate timing and leakage optimization, minimizing iterations. Talus also supports the Common Power Format (CPF) as part of its low-power flow.

### Ensuring Manufacturability at 28 nm

To address design for manufacturability (DFM) and variability issues at 28 nm, [Magma](#) integrates [Talus qDRC](#) physical verification capabilities into the [Talus Vortex](#) place-and-route flow. This solution provides highly accurate timing-driven metal fill that is design-rule clean and meets timing and performance requirements.

Other physical DFM capabilities include lithography hotspot fixing within Talus based on TSMC qualified lithography process check (LPC) hotspot detection engines. By fixing hotspots within the Talus unified design environment, area and timing penalties can be avoided and a design-rule-clean layout is generated. For electrical DFM, TSMC provides an integrated eDFM (electrical DFM) analysis, which is a combination of DFM effects on chemical mechanical polishing (CMP), Thickness-to-Electrical (T2E), lithographic Shape-to-Electrical (S2E), and stress effects. Talus provides complete support for TSMC's eDFM-based timing analysis and optimization.

[Magma](#) Products Qualified for the [TSMC Reference Flow 10.0](#)

Reference Flow 10.0 is supported by [Magma](#)'s full suite of RTL-to-GDSII tools which include:

- Talus Vortex - DFM-aware physical implementation, place-and-route,
- Talus Design - physically-aware RTL synthesis
- Talus Power Pro - low-power design that supports UPF and Common Power Format (CPF)
- Talus qDRC - signoff quality design rule checking, timing-aware metal fill
- Quartz RC - RC extraction

About [Magma](#)

[Magma](#)'s electronic design automation (EDA) software is used to create complex, high-performance integrated circuits (ICs) for cellular telephones, electronic games, WiFi, MP3 players, DVD/digital video, networking, automotive electronics and other electronic applications. [Magma](#) products for IC implementation, analog/mixed-signal design, analysis, physical verification, circuit simulation and characterization are recognized as embodying the best in semiconductor technology, providing the world's top chip companies the "Fastest Path to Silicon."(tm) [Magma](#) maintains headquarters in San Jose, Calif., and offices throughout North America, Europe, Japan, Asia and India. [Magma](#)'s stock trades on Nasdaq under the ticker symbol LAVA. Visit [Magma](#) Design Automation on the Web at [www.magma-da.com](http://www.magma-da.com).

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Forward-looking Statements:

Except for the historical information contained herein, the matters set forth in this press release, including statements about the features and benefits of [Magma](#)'s software and the TSMC Reference Flow 10 and 32/28-nm process technology are forward-looking statements within the meaning of the "safe harbor" provisions of the Private Securities Litigation Reform Act of 1995. These forward-looking statements are subject to risks and uncertainties that could cause actual results to differ materially including but not limited to the ability of [Magma](#)'s and TSMC's products to produce the desired results, the companies' abilities to keep pace with rapidly changing technology and the companies' decisions to continuing working together. Further discussion of these and other potential risk factors may be found in [Magma](#)'s public filings with the Securities and Exchange Commission ([www.sec.gov](http://www.sec.gov)). The company undertakes no additional obligation to update these forward-looking statements.

CONTACT: Magma Design Automation Inc.  
Monica Marmie, Director, Marketing Communications  
(408) 565-7689  
[mmarmie@magma-da.com](mailto:mmarmie@magma-da.com)

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