DATA CENTER DAY
ACCELERATORS DEMYSTIFIED

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TODAY’S DISCUSSION

Accelerators Defined

Implementation Options

Workload Requirements

How Intel Accelerates Key Workloads
WHAT IS AN ACCELERATOR?

Hardware assistance that improves the performance beyond general purpose processing for specific workloads
CUSTOMERS CHOOSE ACCELERATORS TO...

• **Why:** Maximize performance of peak loads

• **When:** Performance / TCO >> general purpose at scale

• **Where:** Portions of specific workloads with routine, stable calculations

• **How:** Offload from CPU cores to adjacent workload-targeted hardware; multiple implementation options
### Silicon Implementation Options

<table>
<thead>
<tr>
<th></th>
<th>Standardized Solution</th>
<th>Customized Solution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processor (CPU)</td>
<td>Product designed for application software with common math &amp; logic operations</td>
<td>Field Programmable Gate Array (FPGA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Merchant product designed for programming custom logic</td>
</tr>
<tr>
<td>Application-Specific Standard Product (ASSP)</td>
<td>Merchant product designed for a specific, common purpose</td>
<td>Application Specific Integrated Circuit (ASIC)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Proprietary silicon designed for a fixed purpose by its user</td>
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Similar to...

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<th>Standardized Solution</th>
<th>Customized Solution</th>
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<tbody>
<tr>
<td>CPU ≈ Word Processor</td>
<td>FPGA ≈ Printing Press</td>
</tr>
<tr>
<td>ASSP ≈ Rubber Stamp</td>
<td>ASIC ≈ Stone Tablet</td>
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</table>

Programmable

Fixed-Function
## Strengths of Each Implementation

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</thead>
<tbody>
<tr>
<td><strong>Programmable</strong></td>
<td><strong>CPU</strong></td>
<td><strong>FPGA</strong></td>
</tr>
<tr>
<td></td>
<td>Best for performance across a broad range of workloads and lowest total cost of ownership</td>
<td>Best for algorithms that are changing and lower R&amp;D investment than ASIC/ASSP</td>
</tr>
<tr>
<td><strong>Fixed-Function</strong></td>
<td><strong>ASSP</strong></td>
<td><strong>ASIC</strong></td>
</tr>
<tr>
<td></td>
<td>Best for fixed-function, stable logic with broad market applicability</td>
<td>Best for proprietary logic with enough value to justify the silicon design investment</td>
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INTEGRATED OR DISCRETE

Discrete chosen to
• maximize configuration flexibility
• improve time to market
• minimize per-chip costs

Integration chosen to
• improve performance
• reduce energy consumption
• minimize system costs
DIVERSE WORKLOAD REQUIREMENTS

Top 3 Growth Workloads

3.7X
Network Core & Wireless

1.8X
Decision Support

1.4X
Digital Content Creation & Delivery

Intel estimates; bubble size is relative CPU intensity
GENERAL PURPOSE XEON PLATFORM PERFORMANCE

1.3-1.5X faster performance each generation

Platform Integration
- e.g. fabrics, photonics, memory, SSDs

New Instructions
- e.g. SIMD, AVX, TSX, AES

Feature Innovations
- e.g. buses, cache, core architecture

Customization
- e.g. custom SoCs, FPGA

Moore’s Law
- e.g. faster transistors, energy efficiency, circuit density
INTEL’S APPROACH TO ACCELERATION

- Optimize Software for IA: e.g. Intel® Data Plane Development Kit
- Discrete Accelerator: e.g. PCIe FPGAs
- Integrated Accelerator: e.g. Intel Iris Pro Graphics
- New IA Instructions: e.g. Advanced Vector Extensions
### Example Usages for FPGA Accelerators

<table>
<thead>
<tr>
<th>Customers</th>
<th>Cloud Service Providers</th>
<th>Security Appliance Vendors</th>
<th>Comms Service Providers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Applications</td>
<td>Image Identification</td>
<td>Security</td>
<td>Firewall, VPN, Router</td>
</tr>
<tr>
<td>Algorithms</td>
<td>Convolutional Neural Network</td>
<td>Encryption</td>
<td>Virtual Switching</td>
</tr>
</tbody>
</table>

1. **Accelerate one application across many servers**
2. **Implement customer-specific solutions**
3. **Reprogram for evolving algorithms**

**Xeon** + **FPGA**
Accelerators are deployed when they provide >> performance/TCO at scale than general purpose CPUs alone

The three typical accelerator implementations are merchant ASSPs, proprietary ASICs, & programmable FPGAs

Intel’s approach is to optimize software for IA, integrate discrete accelerators for key workloads, and add new instructions when the accelerator has broad appeal and is cost effective
THANK YOU!

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