Advancing Moore's Law: Imperatives & Opportunity

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Risk Factors

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If we use any non-GAAP financial measures during the presentations, you will find on our website, intc.com, the required reconciliation to the most directly comparable GAAP financial measure.
“Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate.”

Electronics, Volume 38, Number 8, April 19, 1965
Topics for Today

• Imperatives: What is important
• Breaking through barriers
• What’s next
Imperatives: Cost & Performance

Cost per Transistor

Transistor performance/ generation

- Lower Transistor Leakage
- Higher Transistor Performance (Switching Speed)

* Projected
While Delivering 2 Year Cycles

<table>
<thead>
<tr>
<th>Technology</th>
<th>Date</th>
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<tbody>
<tr>
<td>130 nm</td>
<td>2001</td>
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<td>90 nm</td>
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<tr>
<td>32 nm</td>
<td>2009</td>
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<tr>
<td>22 nm</td>
<td>2011</td>
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Source: Intel
Topics for Today

• Imperatives: What is important
• Breaking through barriers
• What’s next
The End of Scaling is Near?
(Decades of Predictions)

“Optical lithography can’t do sub-micron”

“Optical lithography will reach its limits in the range of 0.75-0.50 microns”

“Optical lithography should reach its limits in the 1990-1994 period”

“X-ray lithography will be needed below 1 micron”

“Minimum geometries will saturate in the range of 0.3 to 0.5 microns”

“Channel lengths can be reduced to approximately 0.2 microns”

“Minimum gate oxide thickness is limited to ~2 nm”

“Oxide reliability may limit oxide scaling to 2.2 nm”

“Plasma etched aluminum will not happen in our lifetime”

“Copper interconnects will never work”

“Scaling will end in ~10 years”

Perceived barriers are meant to be surmounted, circumvented or tunneled through.

Source: ISSCC 2009, The New Era of Scaling in an SoC World, M. Bohr
Innovations Enable Breaking Through Barriers

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<tr>
<th>Year</th>
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<td>High K / Metal Gate</td>
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Source: Intel
Improving Performance through Multiple Innovations

Transistor Performance Trend

Active Power per Function

Benchmarked at constant leakage and constant performance relative to 45nm

Source:
Transistor Performance trend: K. Kuhn, IEDM 2012, Active Power per Function: Intel
The Value of Better Transistors

The Same Fundamental Improvement Benefits a Wide Range of Products

Source: Intel
Cost: the Next Barrier

Such a transition between manufacturing process nodes – without a die footprint shrink as a clear cost saving as a driver – will be a first in the history of IC miniaturization. But Mojy Chian, senior vice president of design enablement, told the International Electronics Forum Thursday (Oct. 4) in a presentation "the normal economics are dead."

Globalfoundries' 14-nm is 'low-shrink' node, Oct. 12, 2012, EE Times, P. Clarke

"No cost/transistor crossover for first time at 28 → 20 nm transition."
Lisa Su, Senior Vice President and GM, Global Business Units, AMD
Heterogeneous Systems Architecture: The next area of computing innovation, ISSCC Keynote, Feb. 18th, 2013

"Chips made at the 14-nm process node may deliver as little as half the typical 30 percent performance increase – and still carry a hefty cost premium – due to the lack of next-generation lithography according to experts speaking at the International Electron Devices Meeting."
IEDM: Moore's Law seen hitting big bump at 14 nm, Dec. 11, 2012, EE Times, R. Merritt

The Clear Focus of the Industry
Competitors May Suffer From No Chip Area Scaling In Future Generations

Competitor Area Scaling (normalized to 28nm)


Intel is continuing to scale while others are pausing to do FinFETs

Intel Area Scaling (normalized to 32nm)
Density Scaling Enables Continued Cost Improvement

Source: Intel
Topics for Today

- Imperatives: What is important
- Breaking through barriers
- What’s next
Innovation-Enabled Technology Pipeline is Full

DEVICES

RELAY

INTEGRATION

STRUCTURE
Leadership: The Right Choices at the Right Time

1999 - Copper Interconnect
   – Skipped 180nm and aligned with mature equipment

200x - SOI Wafers
   – Evaluated extensively, not worth the cost, >$500 million/ generation

2003 - Low-k Interlayer Dielectric
   – Chose CDO vs. SiLK

2003 - SiGe Strained Silicon Transistors
   – Led the way with the right approach

2007 - Immersion Lithography
   – Skipped 45nm and saved >$400 million

2007 - High-k/Metal Gate Transistors
   – Led the way with the right approach

2011 - Tri-Gate Transistors
   – The right path to fully depleted devices

2013 - Wait and See

All that is Needed is Leadership
Summary

• Imperatives
  – Deliver on Cost, Performance/watt, and 2 year cycles

• Breaking through barriers
  – Innovation comes in many forms
  – Continue to invest in research to improve on predicting change

• Opportunity
  – As technology gets harder we can increase our advantages

• The pipeline of ideas is full
  – The challenge is to make the right choices