



White Paper

Intel Architecture and Silicon Cadence

The Catalyst for Industry Innovation

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Introduction

Intel has a long history of setting the pace of industry innovation with the relentless pursuit of Moore's Law. This pace of innovation has served the ever increasing needs of users by providing the ability to increase processor performance, and deliver new features and capabilities, through innovation in processor architecture. As we look at the continuation of this evolution, the industry needs an increased and more predictable pace of innovation to deliver platforms that can provide faster, more connected, trusted, personalized and natural computing experiences. Intel has embarked on a coordinated and accelerated pace of architecture innovation based on its industry-leading silicon expertise, and its architecture design capabilities that will provide the growth driver for the next decade and beyond.

What is Intel Architecture and Silicon Cadence?

Cadence refers to Intel's strategy of introducing a new microarchitecture linked with a new generation of silicon process technology approximately every two years.

Intel's assiduous innovation in silicon technology has enabled the doubling of transistor density approximately every two years, which provides tremendous design flexibility to processor architects to do more. Traditionally, this design flexibility has been used to provide greater performance and features while reducing power. Moving forward the ever evolving

needs of users require even more rapid increases in performance and the convergence of capabilities across blurring usage boundaries. There is therefore the need for a solution architecture that scales across a spectrum of usage segments, and it can be achieved only by industry-wide innovations. Intel's architecture and silicon cadence model provides the innovation engine that will not only drive new processor architectures and chipsets at an established and coordinated pace, but also be the catalyst for industry innovation at a platform level to deliver the benefits of energy efficient performance.

Characteristics of Intel Architecture and Silicon Cadence

The principle of cadence is based on what Intel calls the tick-tock model of silicon and microarchitecture. This model delivers a common processor architecture across all volume market segments. Each “tick” represents the silicon compaction beat rate, and each “tick” has a corresponding “tock” representing the design of a new microarchitecture, delivered in approximately two-year cycles. Intel’s design methodology on a global scale and its tremendous discipline are cornerstones of its principle of cadence which has enabled Intel to deliver innovation in processors and platforms above and beyond the capabilities of the individual products.

An example is the gigantic leap ahead by Intel in scaling the architecture for mobility to deliver server performance. This leap ahead is being delivered by Intel in its processors today. The Intel® Core™2 Duo processor is based on the Intel Core microarchitecture. It has two complete execution cores in one physical processor, both running at the same frequency, and delivers industry-leading energy-efficient performance for mobility as well as the desktop. The computational element of the Intel Core microarchitecture is described as a converged core, which allows optimization of architectures and technologies adapted to usage demands for breakaway performance and energy-efficiency.

Intel is continuing forward on this path of delivering a common scalable architecture based on multi-core processor technologies for servers, desktop and mobile products. The result is an architecture optimized for performance per watt and expanded capabilities on a trajectory of innovation that will propel chipset, interconnect, memory and platform innovations in tick-tock cadence based on a common silicon foundation.

Delivering the Promise

At the heart of delivering the promise of cadence are multiple design teams working together concurrently and in parallel around the world. This requires careful coordination between teams to build on each others’ strengths, complementing each others’ methodologies and plans, with minimal overlap and redundancy.

Intel is also enabling the software community and universities to develop multi-threaded applications, and is playing a catalyst role for the industry ecosystem to take advantage of the pace of innovation. This includes driving standards activities, engagement of the industry and the regulatory environment, and a real commitment to championing user needs.

Cadence is Not New to Intel

In the early 1990s, Intel provided leadership with its IA32 architecture, which established an industry standard and delivered innovation with Intel® Pentium® processors that provided several generations of performance breakthroughs and leadership. The introduction of the Intel Pentium processor in 1993 represented its fifth-generation desktop processor. A slew of innovations then followed: Intel Pentium Pro processor introduced in 1995, the Intel Pentium II in 1997, and the Intel Pentium III in 1999. In 2000, Intel introduced the Intel Pentium 4 processor on the Intel® Netburst® architecture. Intel® Xeon® processors were also introduced in the year 2000.

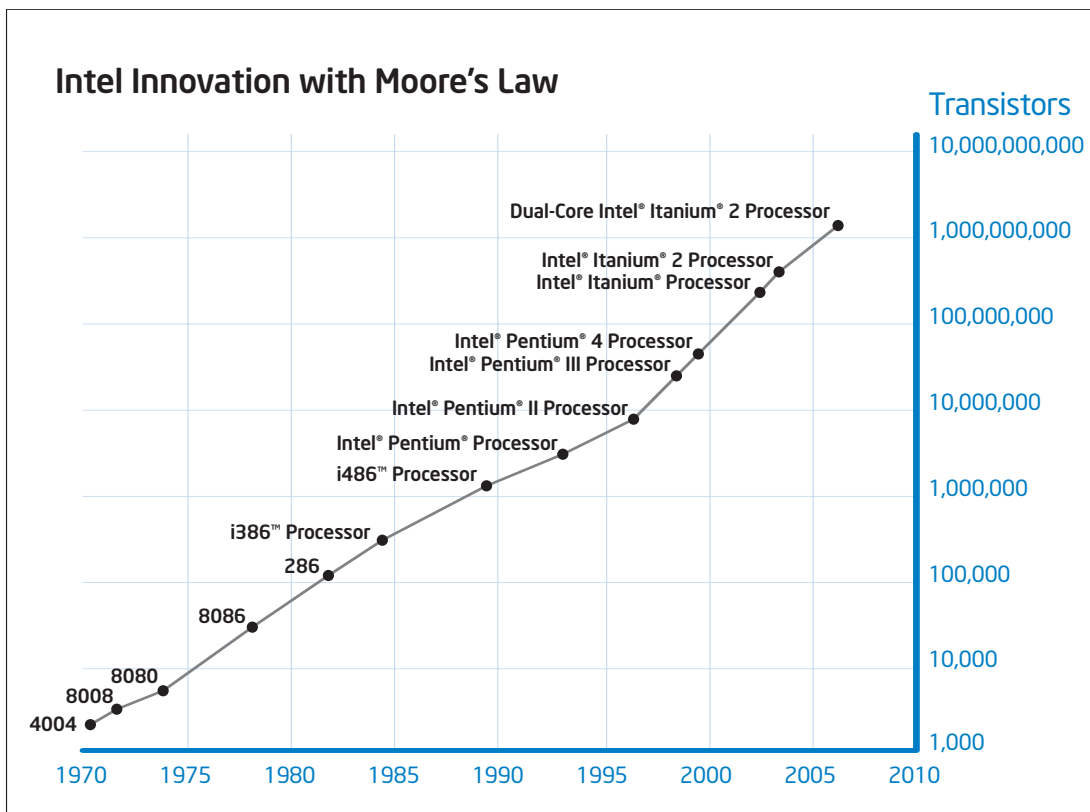
In 2003, the first Intel Pentium M processor on 90nm technology represented a shift to energy-efficient performance, measured in performance per watt, with expanded capabilities. These processor introductions were based on a cadence of silicon innovation, but not necessarily with linked design processes and methodologies.

In 2006, Intel introduced the new Intel® Core™ microarchitecture as the foundation for Intel architecture-based desktop, mobile, and mainstream server multi-core

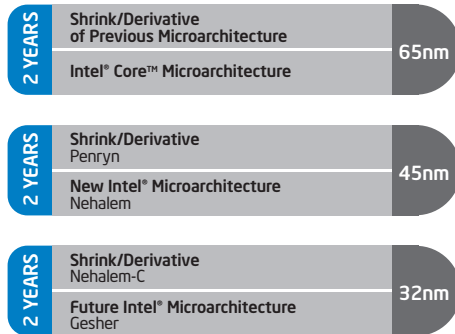
processors. This innovation is based on 65nm process technology and represents the first in an onward trajectory for architecture design linked with silicon innovation in cadence. There are several aspects in Intel's architecture and silicon cadence approach that set it apart from the rest of the industry. These include:

- One microarchitecture for all high-volume market segments, optimized for performance, capabilities and energy efficiency
- Parallel design teams that employ design reuse principles without waiting for the availability of silicon density, but instead drive towards common objectives with linked design goals
- Focus on platform level innovation with parallel chipsets and industry eco-system development for fast ramp of platform capabilities

Intel's cadence model therefore extends its trusted foundation of silicon innovation to deliver industry leading energy-efficient performance architectures at a pace that will fuel industry-wide innovation and growth.



Microprocessor Design Model



Sustained Intel® Technology Leadership

PRINCIPLES

Synchronized silicon and microarchitecture design cadence

One microarchitecture for all high volume market segments

Parallel design teams

No waiting on new process technology

Optimized for energy-efficient performance

Looking into the Future

Intel's future architecture directions will continue to focus on microprocessor core enhancements, delivering performance increases, and building core capabilities with improved energy efficiency. These advancements will continue to deliver compelling thresholds of energy efficient performance that make it feasible for the same processor architecture to be used for mobile, desktop and server computing and execute to the requirements of future applications.

Intel's published roadmap provides a view for the next several generations of silicon process technology with linked architecture introductions. Intel is on track for volume production of Intel Core microarchitecture based products on 45nm in 2007. In 2008 Intel plans to introduce its Nehalem microarchitecture and Geshher in 2010. These microarchitecture introductions will be accompanied with chipset innovations and drive the associated platform ramps

Intel's tick-tock development strategy

The implementation of tick-tock cadence for Intel multi-core processors has been based on the converged core being the fundamental computational element that enables the delivery of targeted performance and capabilities at the right energy efficiency.

Tick-tock therefore requires synchronization of the design processes for the following streams of innovation that correspond with user value across market segments

- Lower power
- Multithread performance
- Features and capabilities
- Increased modularity/flexibility

Key to execution is extending this pace of innovation to industry innovators for true user benefits. Intel has therefore aligned its cadenced steps linked with an overall industry leadership view:

- Eight-quarter compaction technology beat rate ("ticks") synched with an architecture beat rate of eight quarters ("tocks")
- Multiple experienced design teams, concurrently focused on synchronized design goals and milestones, and with process touch points identified for maximizing efficiency
- Frequent "trains" for technology capabilities and features that also provide the ability accommodate change

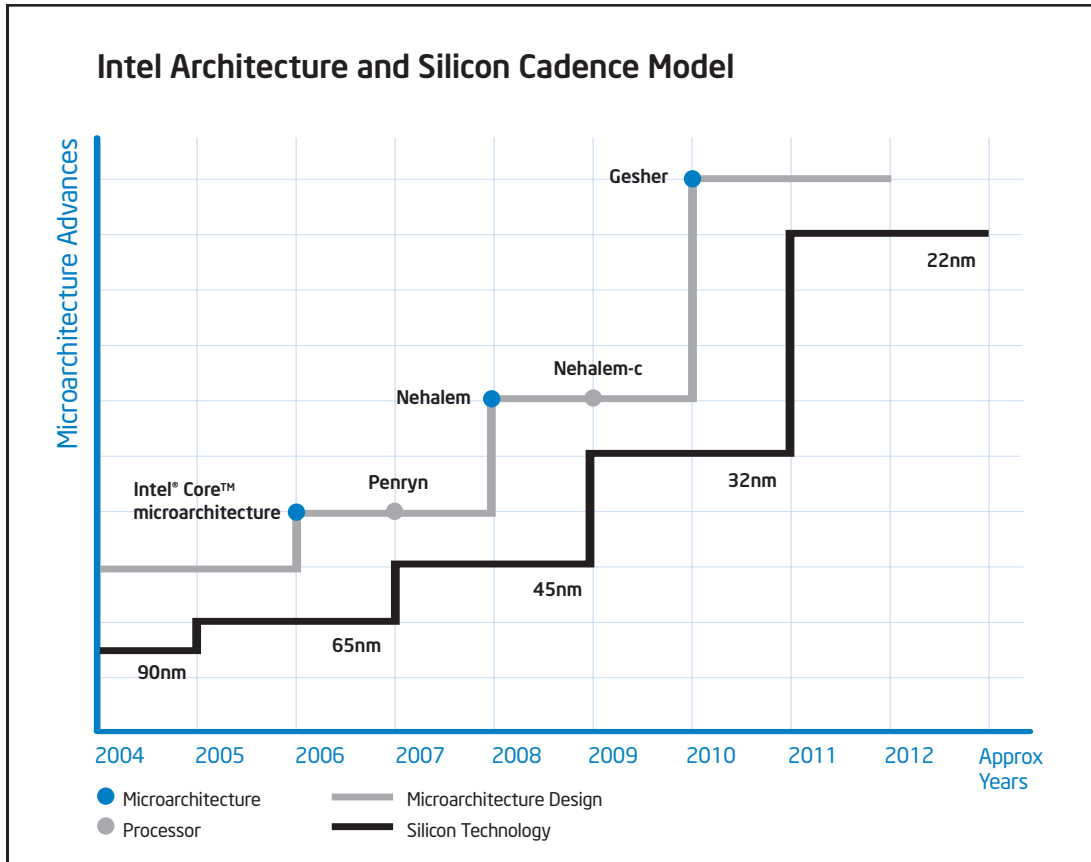
The methodology also encompasses off-beat rate innovations that have bigger implications, with managed risks. This is done with alignment of longer term agendas, building resource profiles and investments for

- Directed research
- Path finding
- Proactive software and platform enablement

A cornerstone of the process is a high level of discipline innate to Intel's culture that will propel innovation, drive milestones linked with the pace of Moore's Law, and ensure that compounding of risks is avoided.

Intel Architecture and Design Methodology

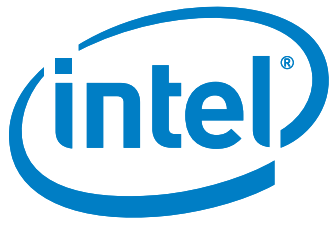
Intel has parallel multi-core processor architecture teams working in tandem with aligned design objectives, milestones and execution mechanisms built in to minimize domino effects. Each of these teams regards the technology beat rate as a cycle for which they have complete ownership. Life-cycle ownership in turn ensures accountability and core competence to meet design deliverables. It also provides better ability to accommodate unanticipated changes. Overall it brings immense creativity and innovation.



Summary

By driving Moore's Law Intel has roughly doubled the number of transistors on a given silicon die approximately every two years. This doubling of transistors offers tremendous design flexibility to provide increased performance, expanded capabilities and improved energy efficiency. In the latest generation of Intel Core microarchitecture products this design flexibility has been utilized to provide enormous performance gains through the addition of cores, stunning features/capabilities for new and improved applications, and remarkable reduction in power. With cadence Intel is driving a trusted and accelerated pace of innovation, delivering a new architecture approximately every two years linked with silicon technology advancements.

Intel's model for tick-tock architecture and silicon cadence represents tremendous gains for the industry and for users, who will benefit with new capabilities and solutions for exponential needs. At Intel we call it a commitment to deliver architecture innovation at the speed of Moore's Law.



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