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Teradyne and Test Insight Partner To Shorten IC Design Cycle Times

Now Offering New Direct EDA To Pattern Solutions

NORTH READING, Mass.--(BUSINESS WIRE)-- Teradyne, Inc. (NYSE:TER) and Test Insight announce the release of new pattern conversion solutions for UltraFLEX to reduce design to test cycle times and expedite Silicon debug and characterization. The new solutions include the ability to compile hundreds of patterns in parallel using Linux-based Load Share Facilities (LSF) as well as the ability to produce binary IG-XL pattern files directly from electronic design automation (EDA) output formats.

The standalone Linux-based compiler can be easily integrated into users' pattern conversion flow. The compiler supports all UltraFLEX digital instruments and triggering of other UltraFLEX instrument families within a digital pattern. The Linux compiler complements the existing Teradyne IG-XL Windows compiler for bulk conversion tasks by enabling the use of a customer's Linux based compute farm resources, which are typically used by design and DFT engineers, to generate test programs. The product has been tested and validated by several large customers and is now available for all users.

The Test Insight Tool Suite has also been updated to allow the generation of IG-XL binary pattern files directly from STIL/WGL/VCD to Teradyne UltraFLEX IG-XL binary formats within the ATEGEN toolset. It reduces the complexity of pattern conversion to a single step process by leveraging the Linux pattern compiler and the rich feature set of the Test Insight Tool Suite for pattern conversion. "The tight cooperation with Teradyne helps us improve our software solutions and keep up with the latest needs of most advanced users in semiconductor test," said Meir Gellis, CEO of Test Insight.

"Our customers are under increasing pressure to ramp their complex System-on-a-Chip (SOC) devices as soon as samples are available. Device data volumes typically exceed 100GB per device and these volumes have traditionally grown by 15-20% per device generation. During early ramp, test vectors can be fully regenerated 10-20 times, which presents test engineers with a computational bottleneck during the critical debug chip period. The Linux compiler enables our customers to compile hundreds of GBs in minutes by leveraging customers' existing compute farms. This will enable UltraFLEX customers to ramp their products faster, allowing more time to debug critical device issues," noted Gregory Smith, Vice President of SOC Marketing at Teradyne.

About Test Insight

Test Insight Ltd. puts years of test engineering experience into innovative software tools that provide better integration between design and test. Using an innovative process, Test Insight software solutions allow engineers to accomplish better results, easier and with higher quality. Building on vast test engineering experience and adding cutting edge sophisticated software development makes Test Insight products and technology stand out in quality and performance. For further information, contact us at info@testinsight.com or visit www.testinsight.com.

About Teradyne

Teradyne (NYSE:TER) is a leading supplier of Automatic Test Equipment used to test semiconductors, wireless products, data storage and complex electronic systems which serve consumer, communications, industrial and government customers. In 2013, Teradyne had sales of $1.43 billion and currently employs approximately 3,800 people worldwide. For more information, visit www.teradyne.com.

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