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Highly Integrated, Low-Power Clock ICs from Silicon Labs Simplify Timing for Demanding 10/25/100G Designs

-- New Si5332 Family Offers Best-in-Class Clock Tree Consolidation, Replacing Multiple Oscillators, Buffers and Clock ICs --

AUSTIN, Texas, Sept. 25, 2017 /PRNewswire/ -- Silicon Labs (NASDAQ: SLAB) has introduced a new family of high-performance clock generators offering the industry's most highly integrated timing solution for 10/25/100G applications. The new Si5332 clock family leverages Silicon Labs' proven MultiSynth fractional clock synthesis technology to deliver a timing solution that provides best-in-class frequency flexibility and jitter performance of 230 fs rms. Multiple Si5332 options spanning 6, 8 and 12 clock outputs enable clock tree consolidation for demanding applications including hyperscale data center switches, servers, storage, networking, small cells, broadband, broadcast video, multi-function printers and industrial applications.

Complex devices such as Ethernet switches, high-speed switch fabrics, network processors, server SoCs and FPGAs combine data path processing, CPU functions and multiple serializers/deserializers (SerDes) into a single IC. As a result, these devices require a diverse combination of reference timing. 10/25/100G SerDes have stringent jitter requirements, often requiring clocks with < 300 fs rms maximum jitter performance. CPU phase-locked loops have lower jitter requirements but often use spread spectrum clocking to minimize electromagnetic interference (EMI). Unlike traditional timing solutions that use a mix of crystal oscillators, buffers and fixed-frequency clock generators, Si5332 clocks generate all SerDes, processor and system clocks in a single-chip device while providing significant jitter margin, enabling system developers to simplify clock trees and design with confidence.

"Hyperscale data centers are quickly migrating from 10G to 25G, 50G and 100G Ethernet to accelerate data transfer and network efficiency. This new investment cycle is spurring equipment manufacturers to upgrade switch and access ports to higher speeds and to adopt higher performance timing solutions," said James Wilson, Senior Marketing Director for Silicon Labs' timing products. "By choosing Silicon Labs' Si5332 any-frequency clocks, system designers can optimize their clock tree designs without compromising timing performance."

The Si5332 family is optimized to provide reference timing for the high-speed serial interconnects used in next-generation data centers. The new product family supports PCI Express (PCIe), the long-term dominant standard for interconnecting microprocessors, networking, storage and memory. The Peripheral Component Interconnect Special Interest Group (PCI-SIG) recently introduced PCI Express 4.0 (revision 0.9), which supports 16 gigatransfers per second (GT/s) data rates. The Si5332 family fully complies with PCI Express 4.0 while providing 60 percent jitter margin to PCIe Gen 4 specifications.

Other industry consortia, including CCIX, Gen-Z, NVLink and OpenCAPI, are working on alternate serial interconnect technology supporting speeds up to 25 GT/s. In addition to requiring low jitter clocks, some of these solutions require spread spectrum reference clocks. The Si5332 family provides a versatile solution supporting dual independent spread spectrum paths. Spread spectrum clock generation is enabled on a per output basis, enabling a single clock device to

simultaneously support a mix of spread and non-spread clocks. Collectively, these features make the Si5332 family the best solution to provide reference timing for high-speed serial interconnects.

Si5332 clock generators are purpose-built to simplify clock tree design without compromising performance or power. The new family combines two MultiSynth fractional clock synthesizers and five independent integer dividers, eliminating the need for fixed-frequency clocks and oscillators for clock generation. With jitter performance of 230 fs rms, Si5332 clocks offers 2x to 5x lower jitter than competing solutions while providing margin to 10/25/100G SerDes timing requirements. Si5332 clocks integrate extensive on-chip power supply regulation, eliminating the need for expensive discrete low-dropout (LDO) regulators required by competing solutions. The Si5332 family's MultiSynth-based architecture is similarly optimized for power efficiency, with 50 to 60 percent lower power than competing solutions.

Each Si5332 clock output can be configured as LVPECL, LVDS, HCSL or LVCMOS and supports 1.8 to 3.3 V, eliminating the need for discrete format or voltage translators and simplifying interfacing to FPGAs, ASICs and SoCs. In addition to I2C control, the clocks support user-defined control pins that can be used to quickly configure each device without the need of a serial interface. Like other Silicon Labs timing products, the Si5332 clocks are configurable and customizable using flexible ClockBuilder Pro software.

Pricing and Availability
Samples and production quantities of the Si5332 any-frequency clocks are available now. Samples ship in two weeks, and production quantities are available in four weeks. Pricing in 10,000-unit quantities starts from $4.25 (USD) for the 6-output device to $4.90 (USD) for the 12-output clock. Silicon Labs' new Si5332-6EX-EVB, Si5332-8EX-EVB and Si5332-12EX-EVB development kits, priced at $149 each (USD MSRP), provide quick, simple device evaluation. For more information about the Si5332 clock family or to order samples and development kits, visit www.silabs.com/si5332-any-frequency-clocks.

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